STRING DIAGRAM SEMANTICS OF DIGITAL CIRCUITS

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joint work with Achim Jung and Aliaume Lopez

Synchron 2019 @ Aussois

UNIVERSITY OF BIRMINGHAM

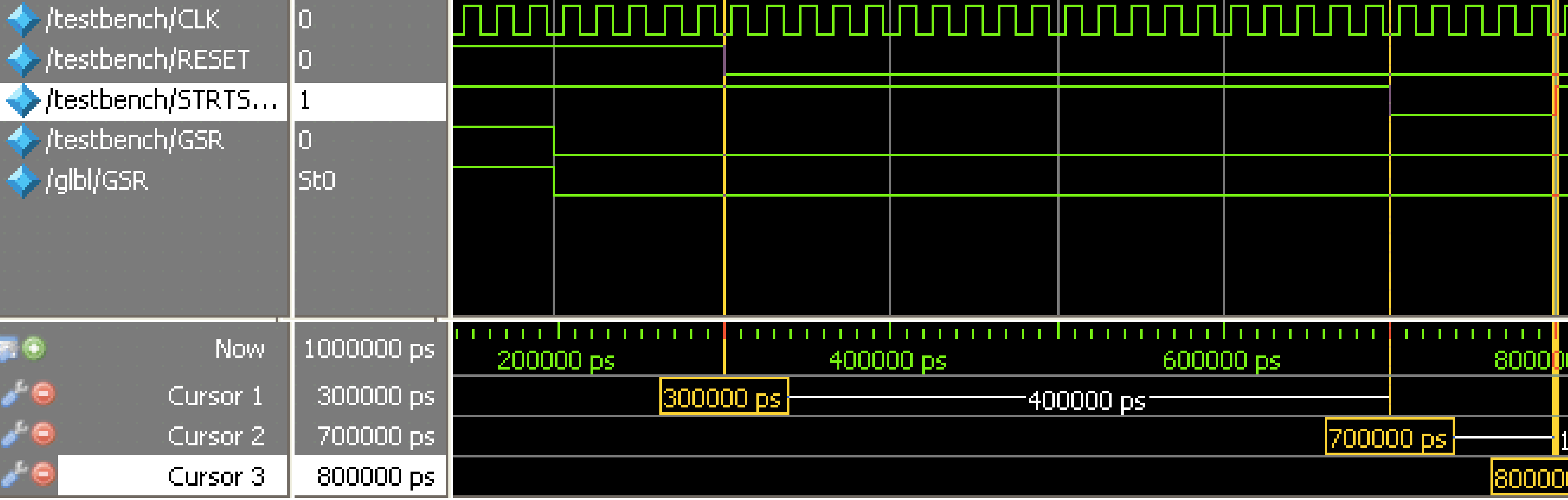
FMCAD'17 // CSL'18

The Geometry of Synthesis

VERITYGOS.ORG

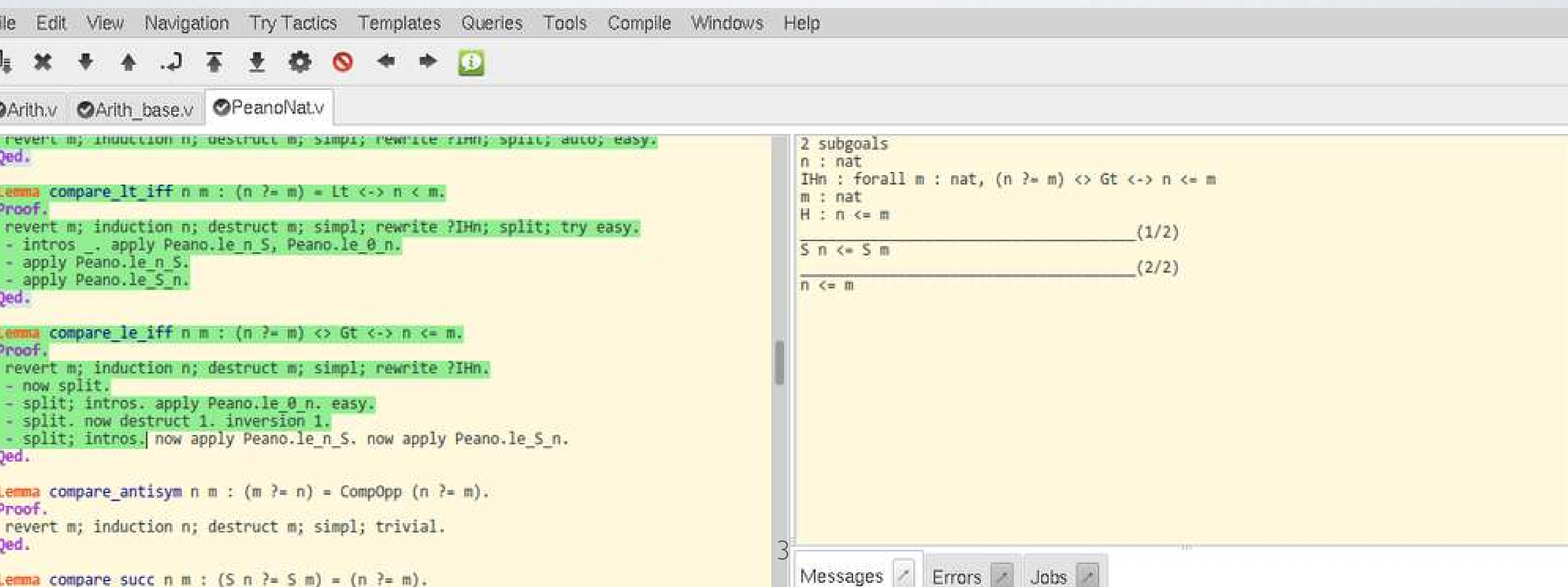
$\lambda \mapsto$

POPL'07 // POPL'11 // ICFP'11



/testbench/CLK 0
/testbench/RESET 0
/testbench/STRTS... 1
/testbench/GSR 0
/glbl/GSR St0
Now 1000000 ps
Cursor 1 300000 ps
Cursor 2 700000 ps
Cursor 3 800000 ps
200000 ps
400000 ps
600000 ps
300000 ps
400000 ps
700000 ps

vs



Edit View Navigation Try Tactics Templates Queries Tools Compile Windows Help
Arith.v Arith_base.v PeanoNat.v
Lemma compare_lt_iff n m : (n ?= m) = Lt <-> n < m.
Proof.
revert m; induction n; destruct m; simpl; rewrite ?IHn; split; try easy.
- intros _. apply Peano.le_n_S, Peano.le_0_n.
- apply Peano.le_n_S.
- apply Peano.le_S_n.
Qed.
Lemma compare_le_iff n m : (n ?= m) <> Gt <-> n <= m.
Proof.
revert m; induction n; destruct m; simpl; rewrite ?IHn.
- now split.
- split; intros. apply Peano.le_0_n. easy.
- split. now destruct 1. inversion 1.
- split; intros. now apply Peano.le_n_S. now apply Peano.le_S_n.
Qed.
Lemma compare_antisym n m : (m ?= n) = CompOpp (n ?= m).
Proof.
revert m; induction n; destruct m; simpl; trivial.
Qed.
2 subgoals
n : nat
IHn : forall m : nat, (n ?= m) <> Gt <-> n <= m
m : nat
H : n <= m
(1/2)
S n <= S m
(2/2)
n <= m
Messages Errors Jobs

SYNTACTIC REASONING

- formalisation
- manipulating open terms
- partial evaluation // supercompilation
- symbolic execution // abstract interpretation
- success story in PLs: opsem // types // logics

CAN WE REASON

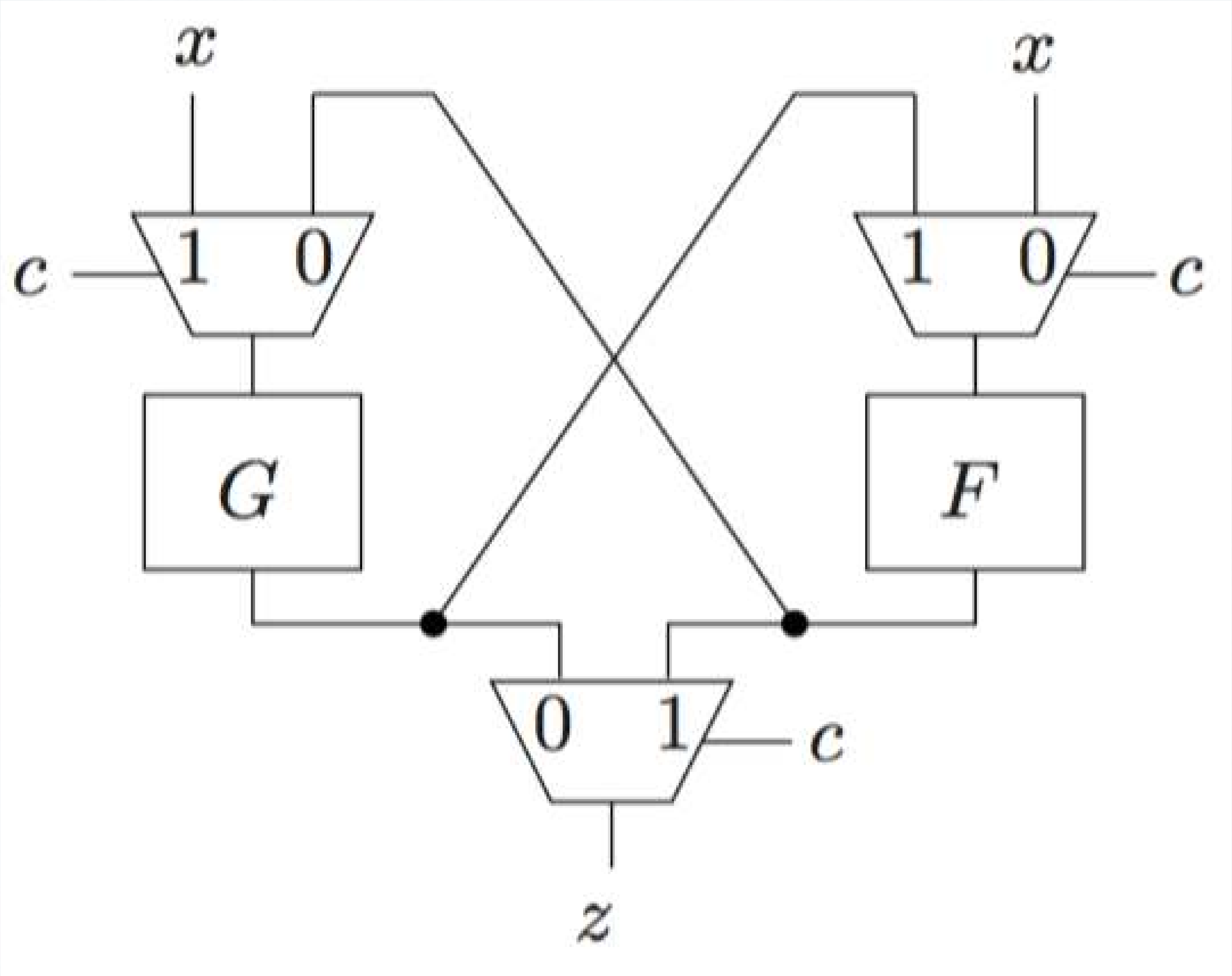
EQUATIONALLY

SYNTACTICALLY

OPERATIONALLY

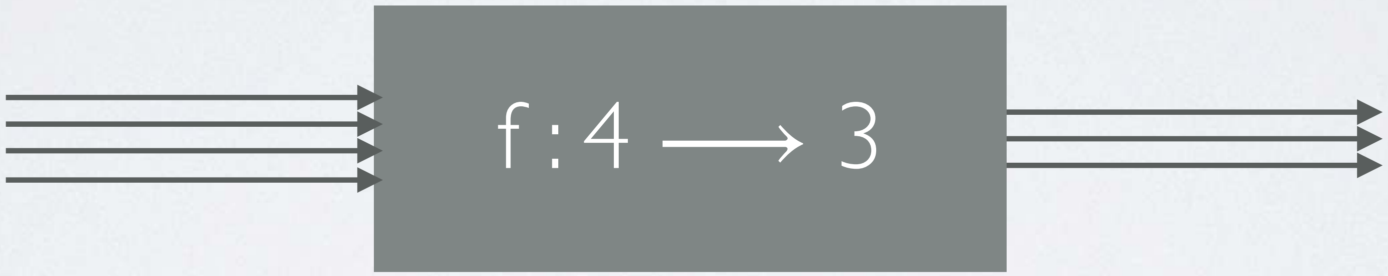
ABOUT CIRCUITS?

COMBINATIONAL FEEDBACK

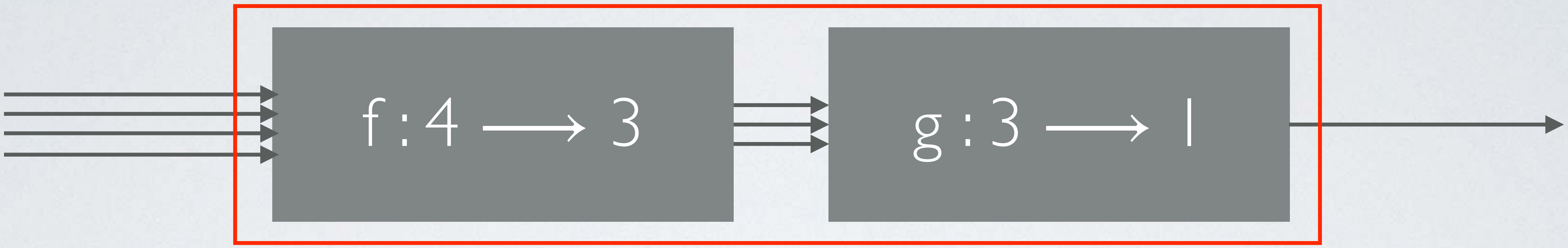


if c **then** F(G(x)) **else** G(F(x))

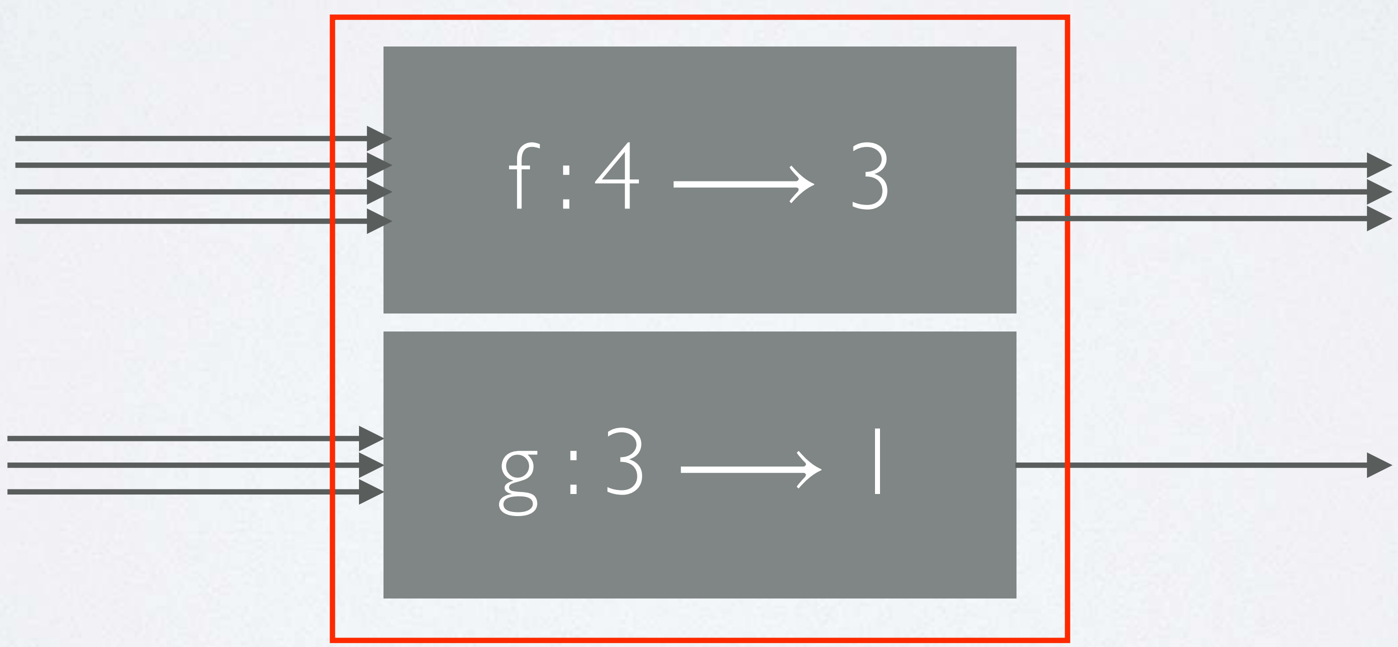
STRING DIAGRAMS



COMPOSITION



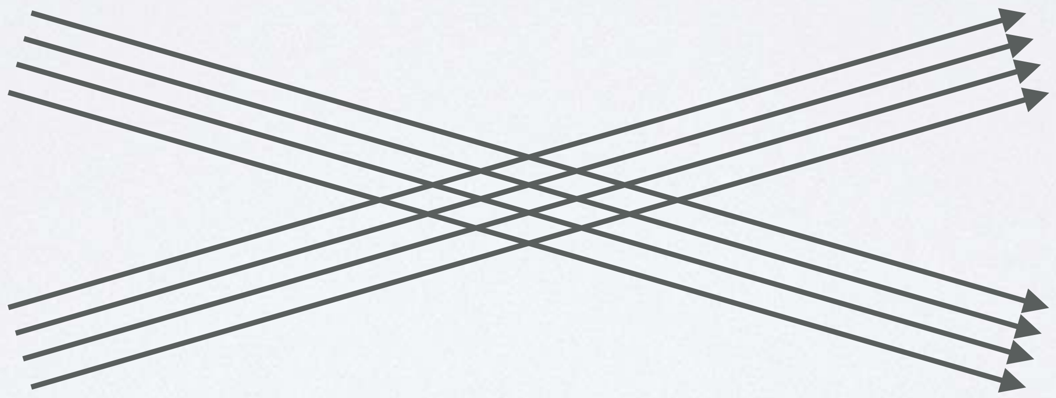
$f \cdot g : 4 \longrightarrow 1$



$f \otimes g : 7 \longrightarrow 4$

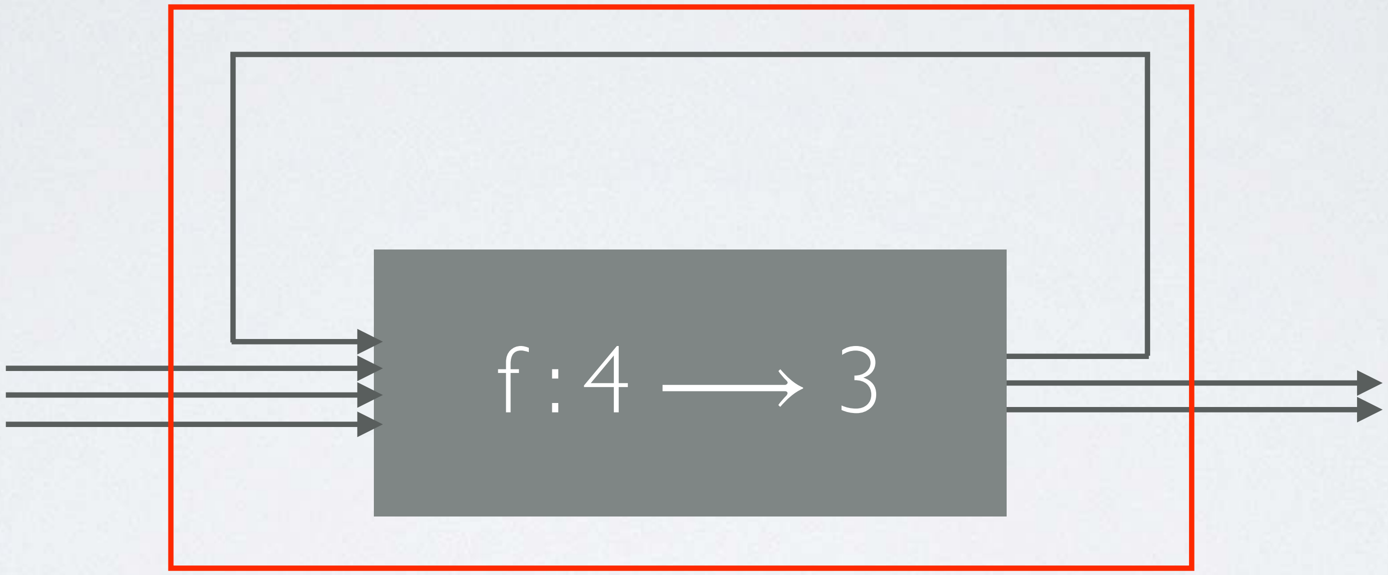
IDENTITY AND SYMMETRY

$\mathrm{id}_4 : 4 \longrightarrow 4$



$\gamma_4 : 8 \longrightarrow 8$

TRACE



$Tr\,(f) : 3 \longrightarrow 3$

SOUND AND COMPLETE EQUATIONAL SYSTEM

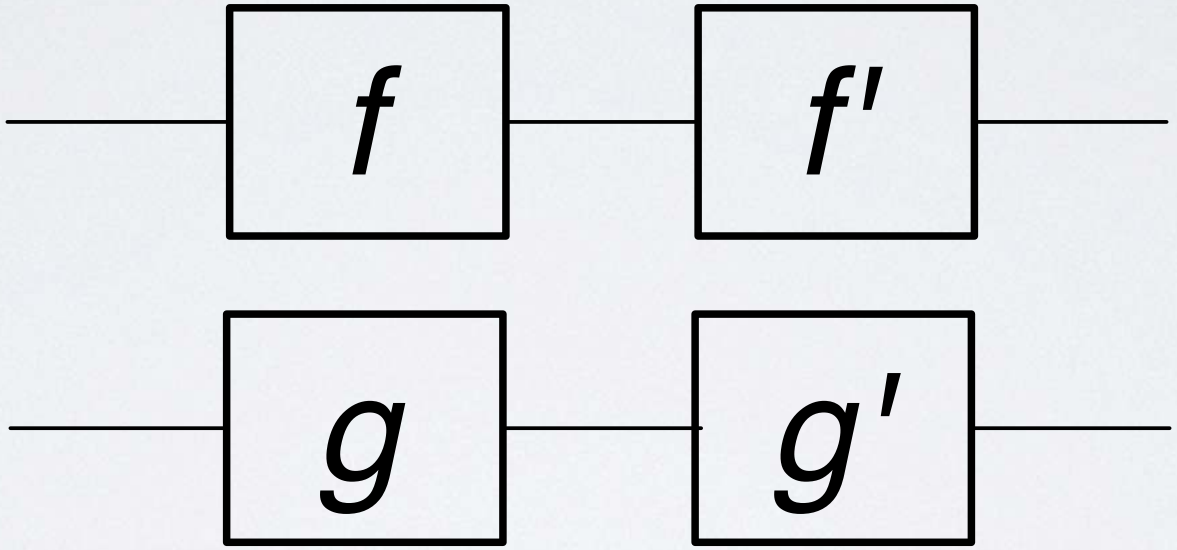
STRICT SYMMETRIC TRACED MONOIDAL CATEGORY

$\simeq$

GRAPHS*

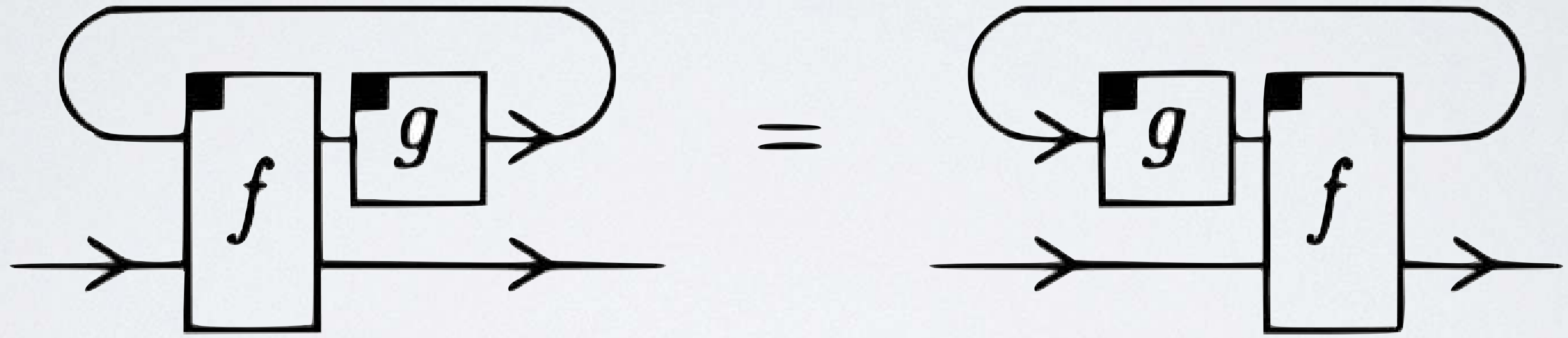
* Monoidal hypergraphs.

EXAMPLE OF EQUATION



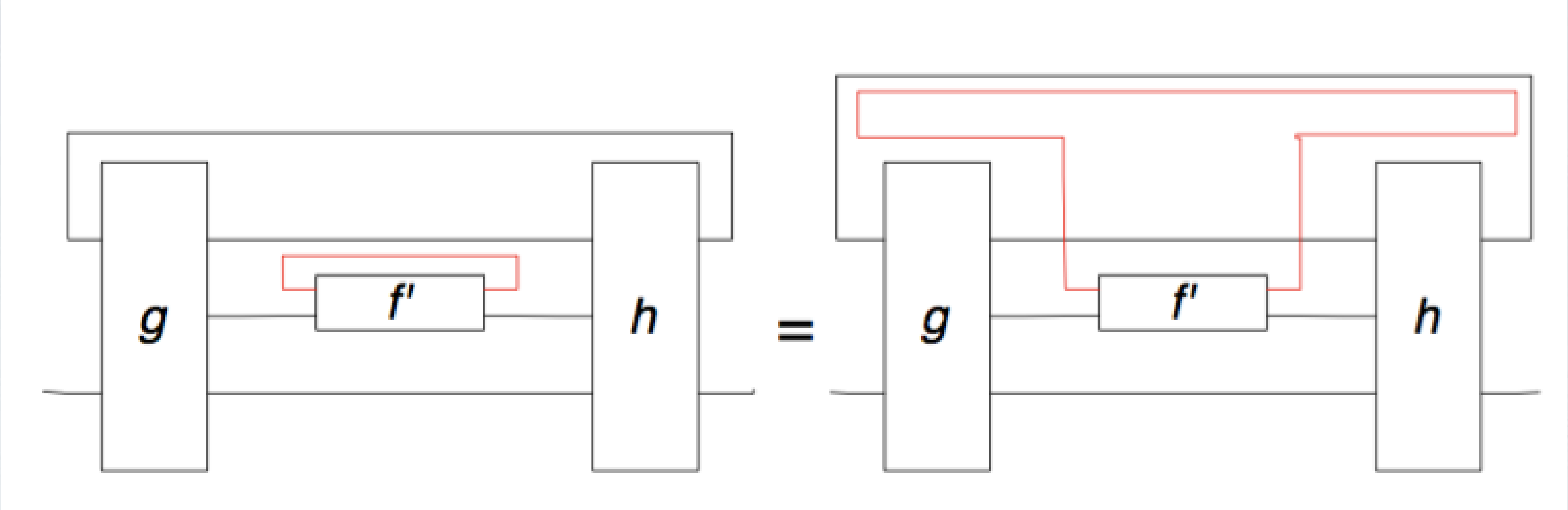
$$(f \cdot f') \otimes (g \cdot g') = (f \otimes g) \cdot (f' \otimes g')$$

EXAMPLE OF EQUATION



$Tr(f \cdot (g \otimes n)) = Tr((g \otimes m) \cdot f)$

EXAMPLE OF PROPOSITION

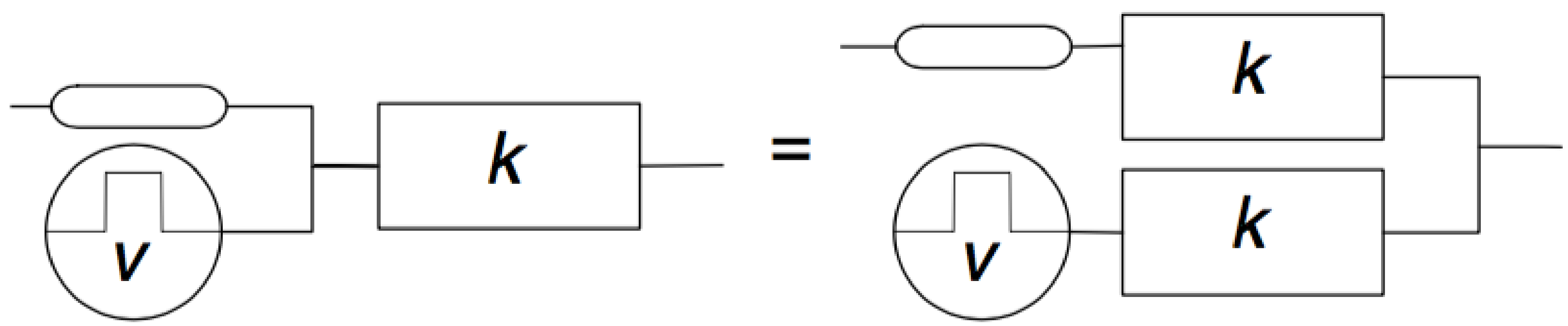


$$\mathrm{Tr}^q\big(g \cdot (m \otimes \mathrm{Tr}^p(f') \otimes n) \cdot h\big) = \mathrm{Tr}^{p+q}\big((p \otimes g) \cdot (\mathsf{x}_{p,m} \otimes r) \cdot f' \cdot (\mathsf{x}_{m,p} \otimes r) \otimes n) \cdot (p \otimes h)\big)$$

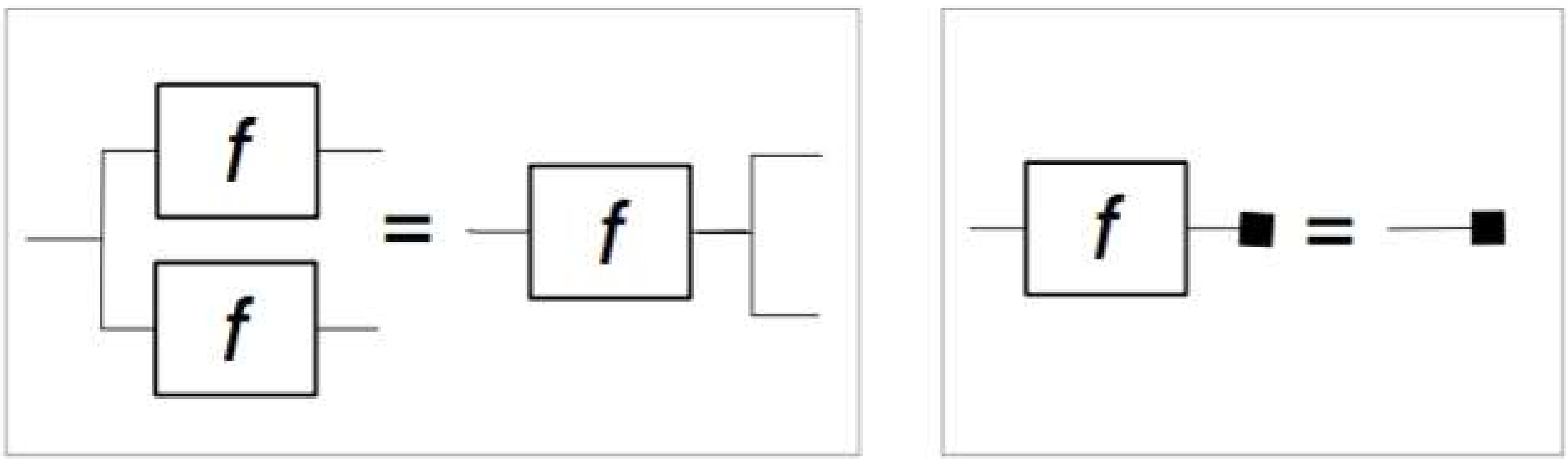
Equational ≃ Diagrammatic

SMALL AXIOMS

Streaming: *For any levels* $\mathbf{v} = v \otimes v'$ *and gate* k, $(\delta^2 \otimes \mathbf{v}) \cdot \nabla_2 \cdot k = ((\delta^2 \cdot k) \otimes (\mathbf{v} \cdot k)) \cdot \nabla_1$.

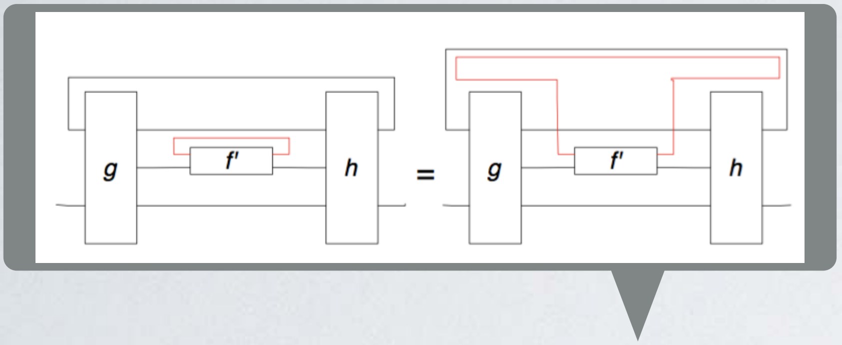


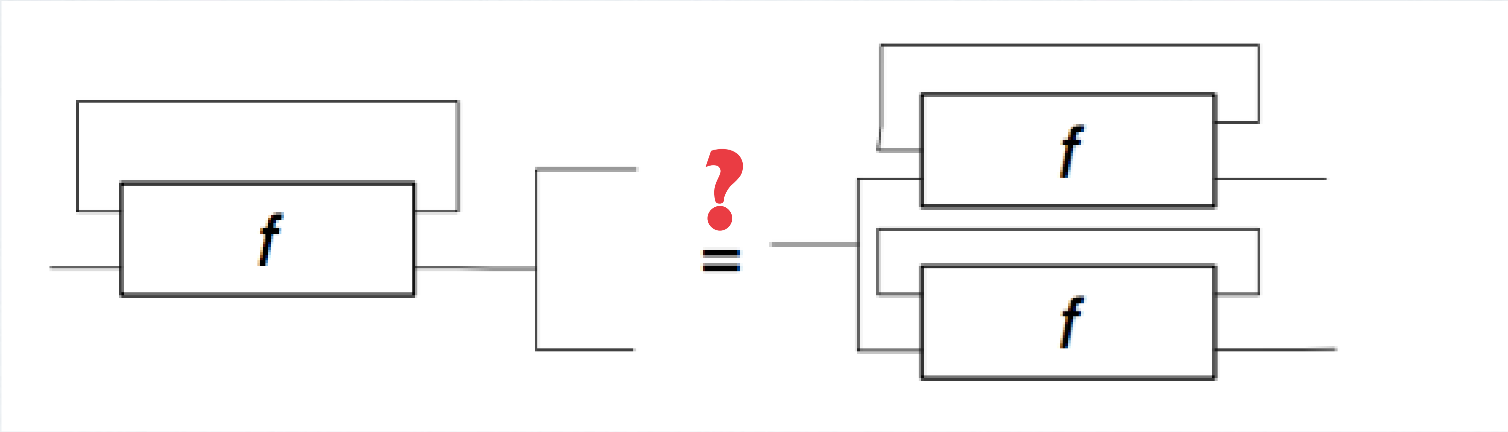
CARTESIAN PRODUCT



$$\langle f, f \rangle = \Delta_n \cdot (f \otimes f) = f \cdot \Delta_m \qquad f \cdot \mathsf{w}^m = \mathsf{w}^m.$$

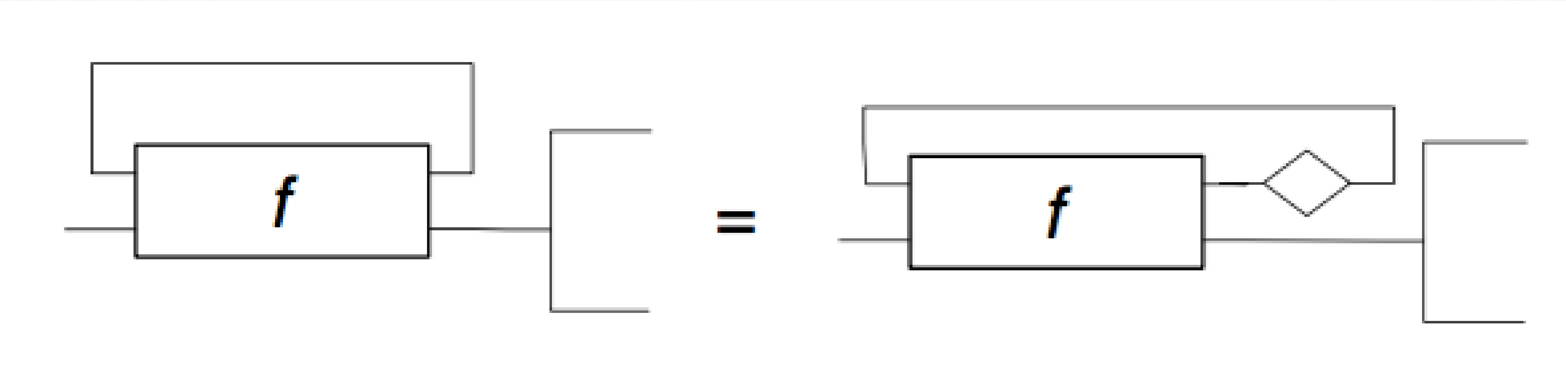
DIAGRAMMATIC PROOF





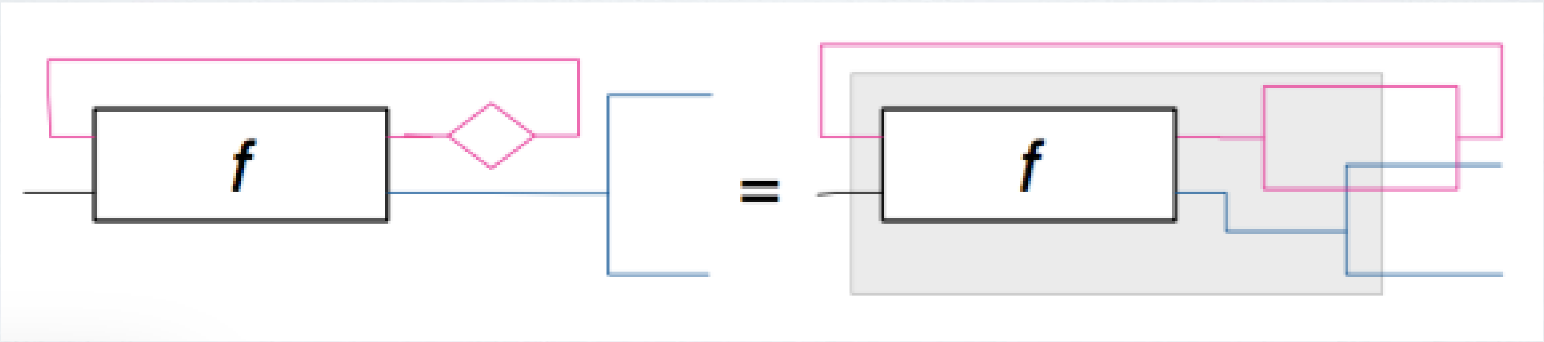
induction

DIAGRAMMATIC PROOF



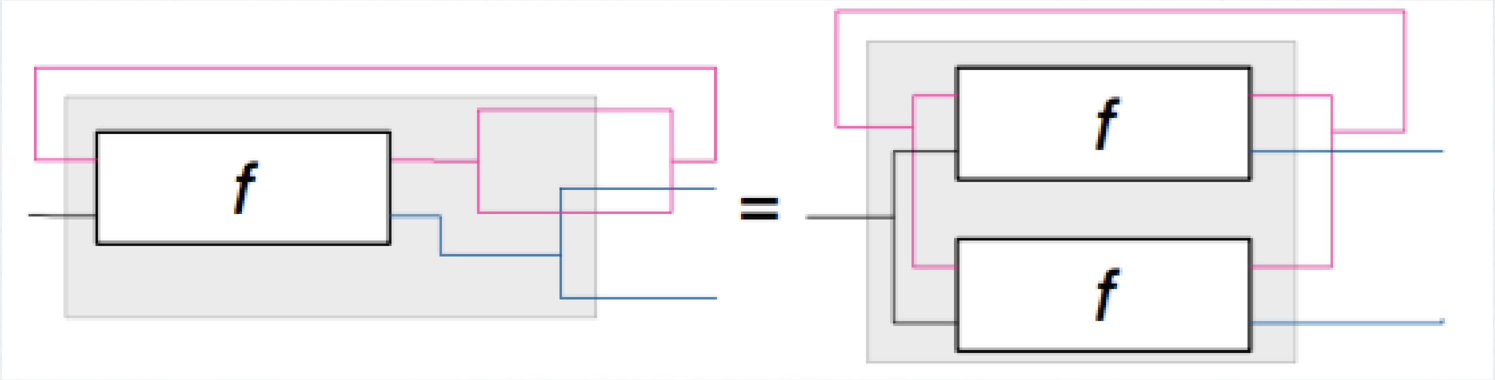
$f \cdot j = 1$

DIAGRAMMATIC PROOF



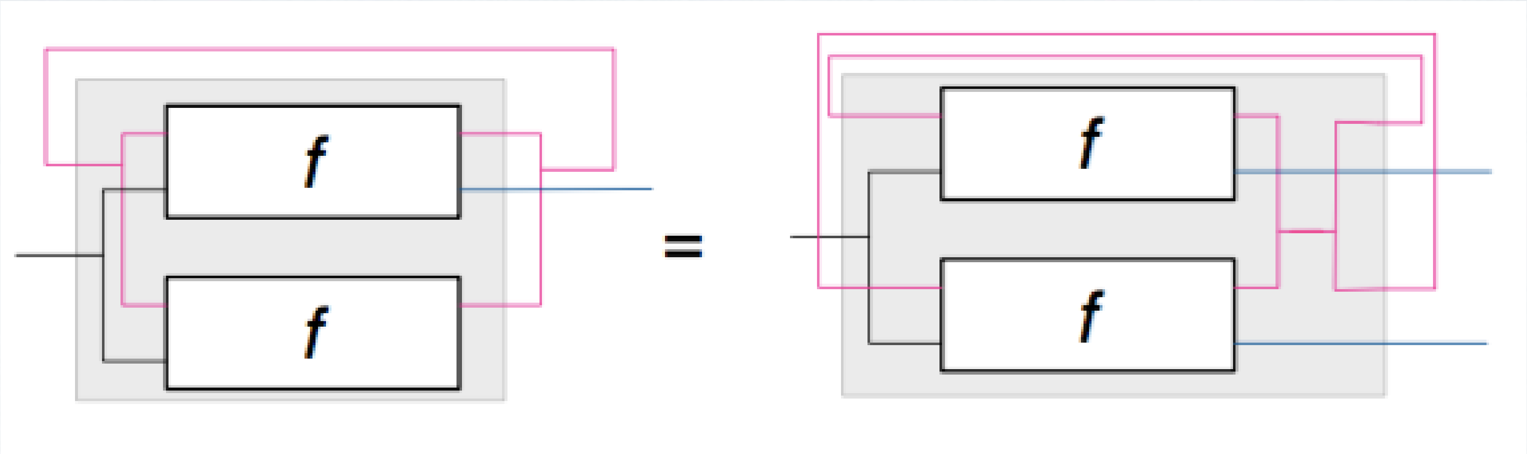
diagrammatic reasoning

DIAGRAMMATIC PROOF



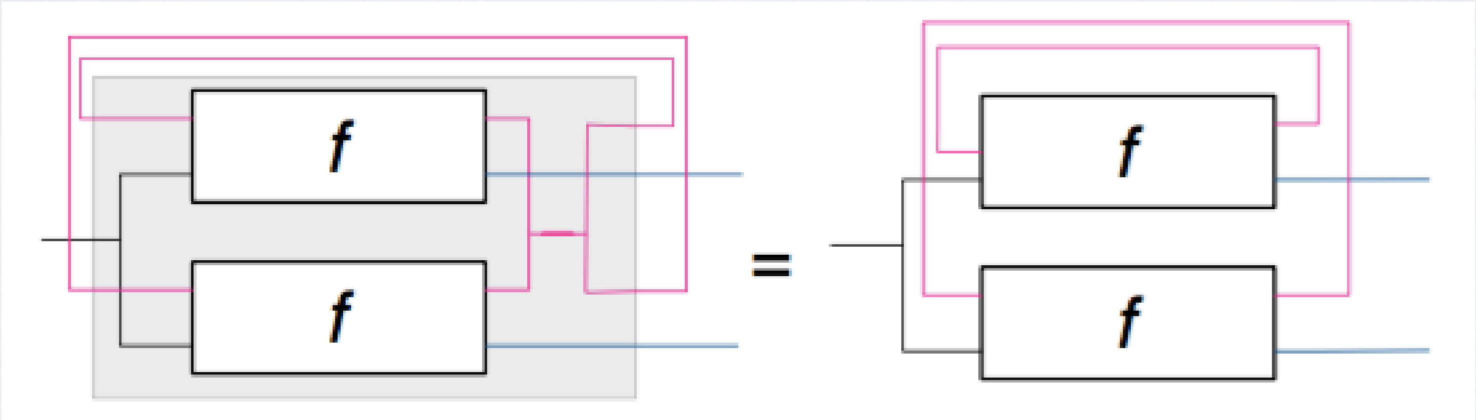
induction hypothesis

DIAGRAMMATIC PROOF



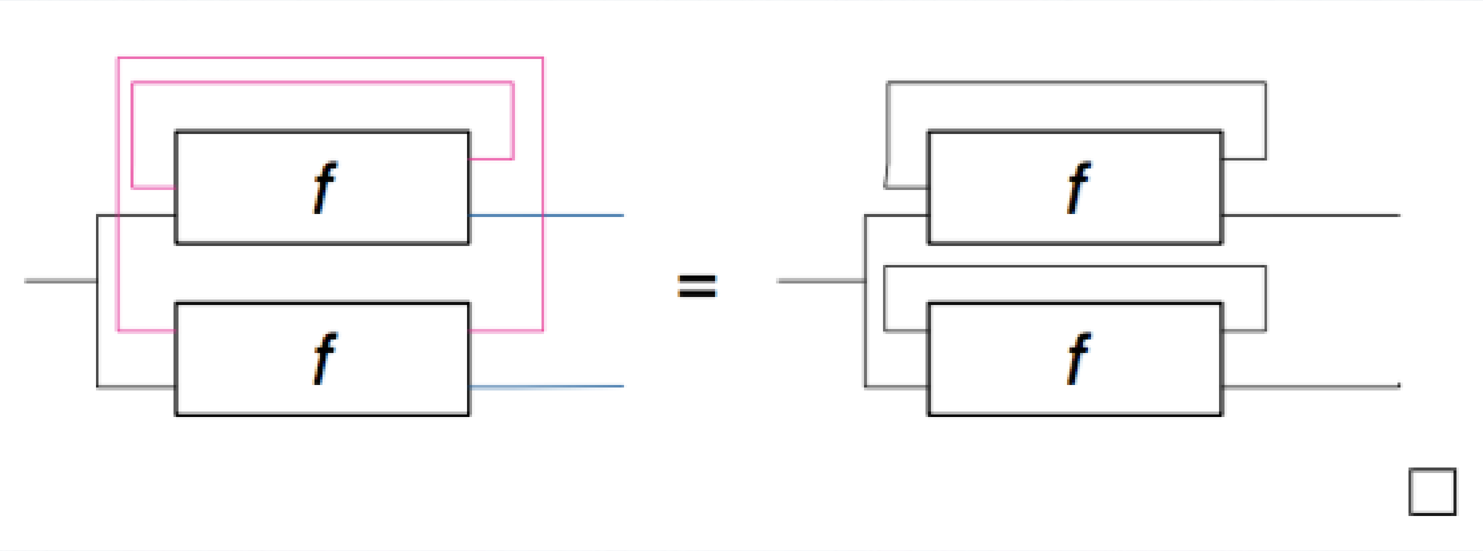
diagrammatic reasoning

DIAGRAMMATIC PROOF



corollary of determinism (separate proof)

DIAGRAMMATIC PROOF



diagrammatic reasoning

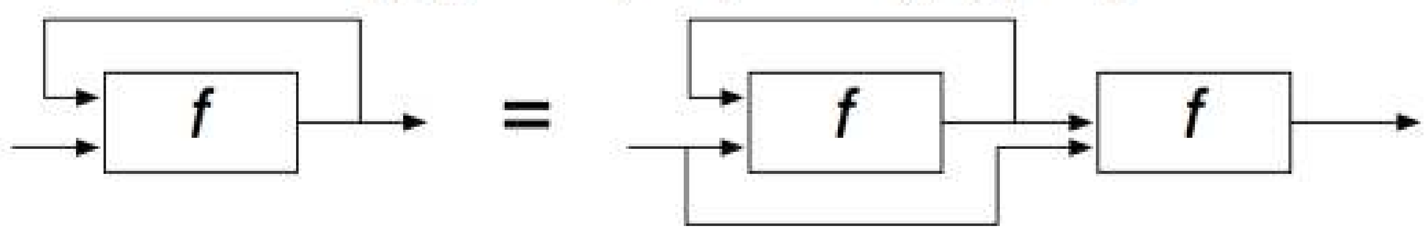
EQUATIONS ⇒ SPECS

DIAGRAMS ⇒ CALCULATIONS

TRACE + PRODUCT = ITERATION

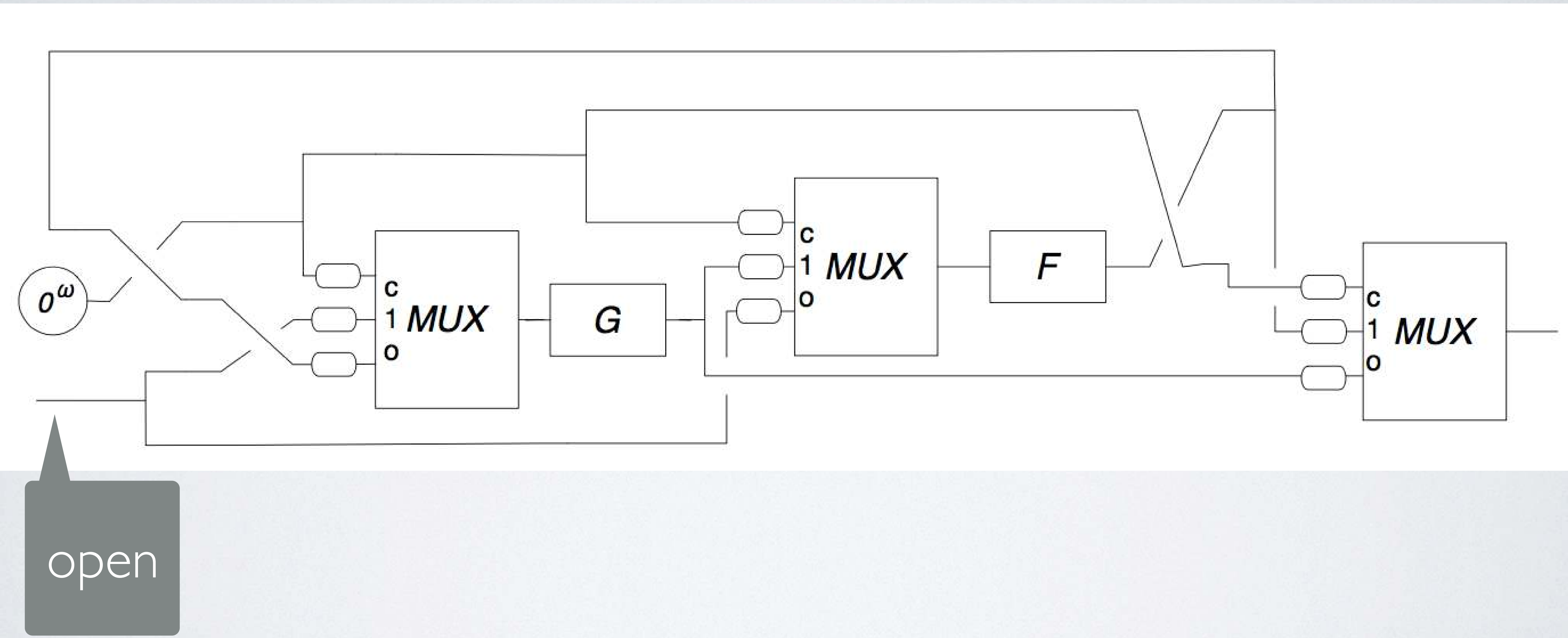
$$\mathrm{iter}^n(f) = \mathrm{Tr}^n(f \cdot (\Delta_n \otimes n)) : m \to n$$

Iteration: $\mathrm{iter}(f) = \langle m, \mathrm{iter}(f) \rangle \cdot f$

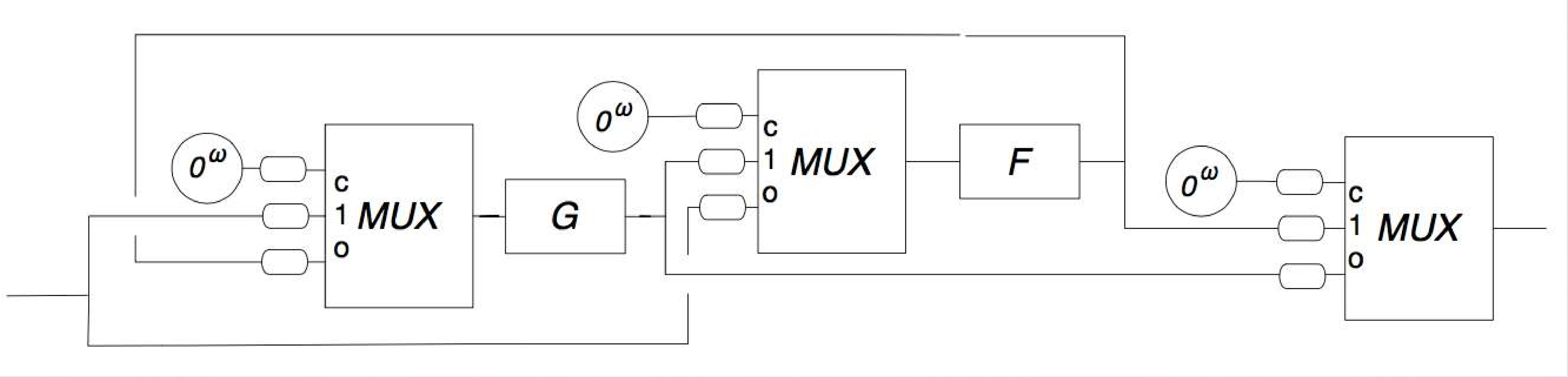


Cazanescu and G. Stefanescu // Hasegawa1990

COMBINATIONAL FEEDBACK

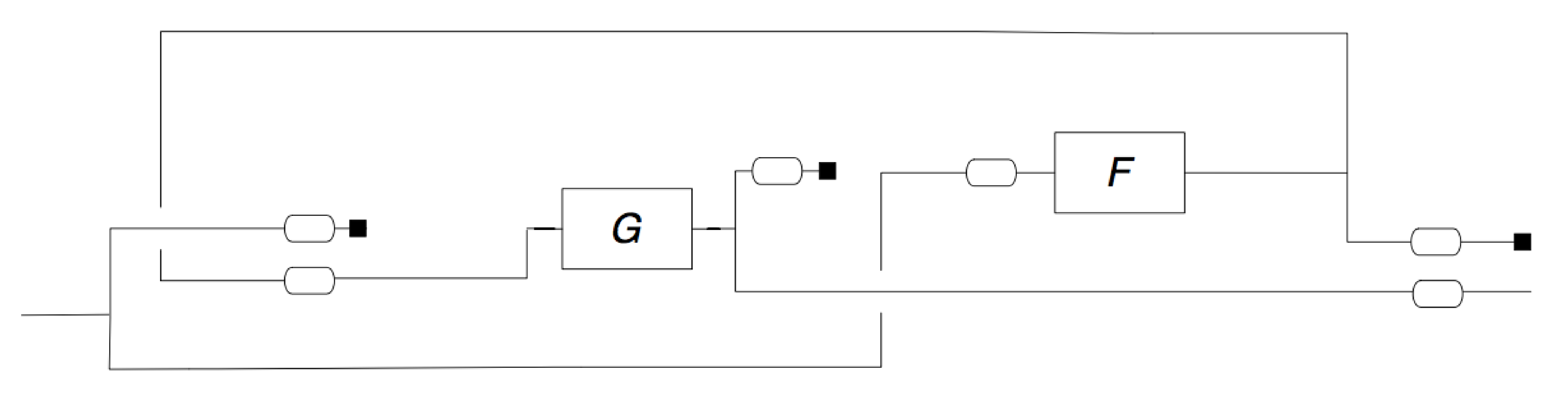


COMBINATIONAL FEEDBACK



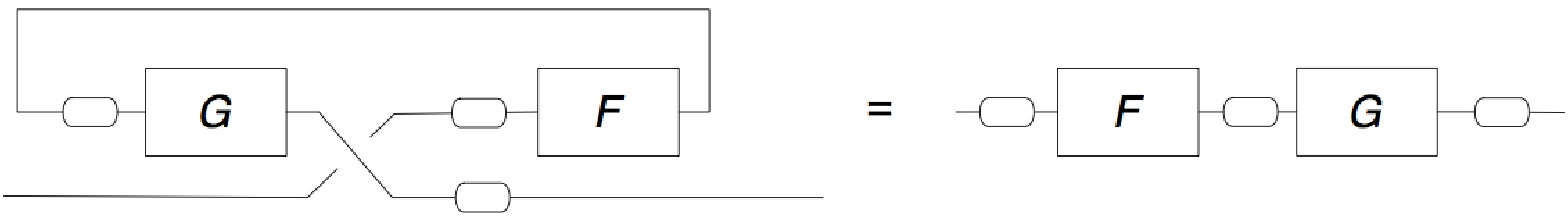
Copy the 0 stream

COMBINATIONAL FEEDBACK



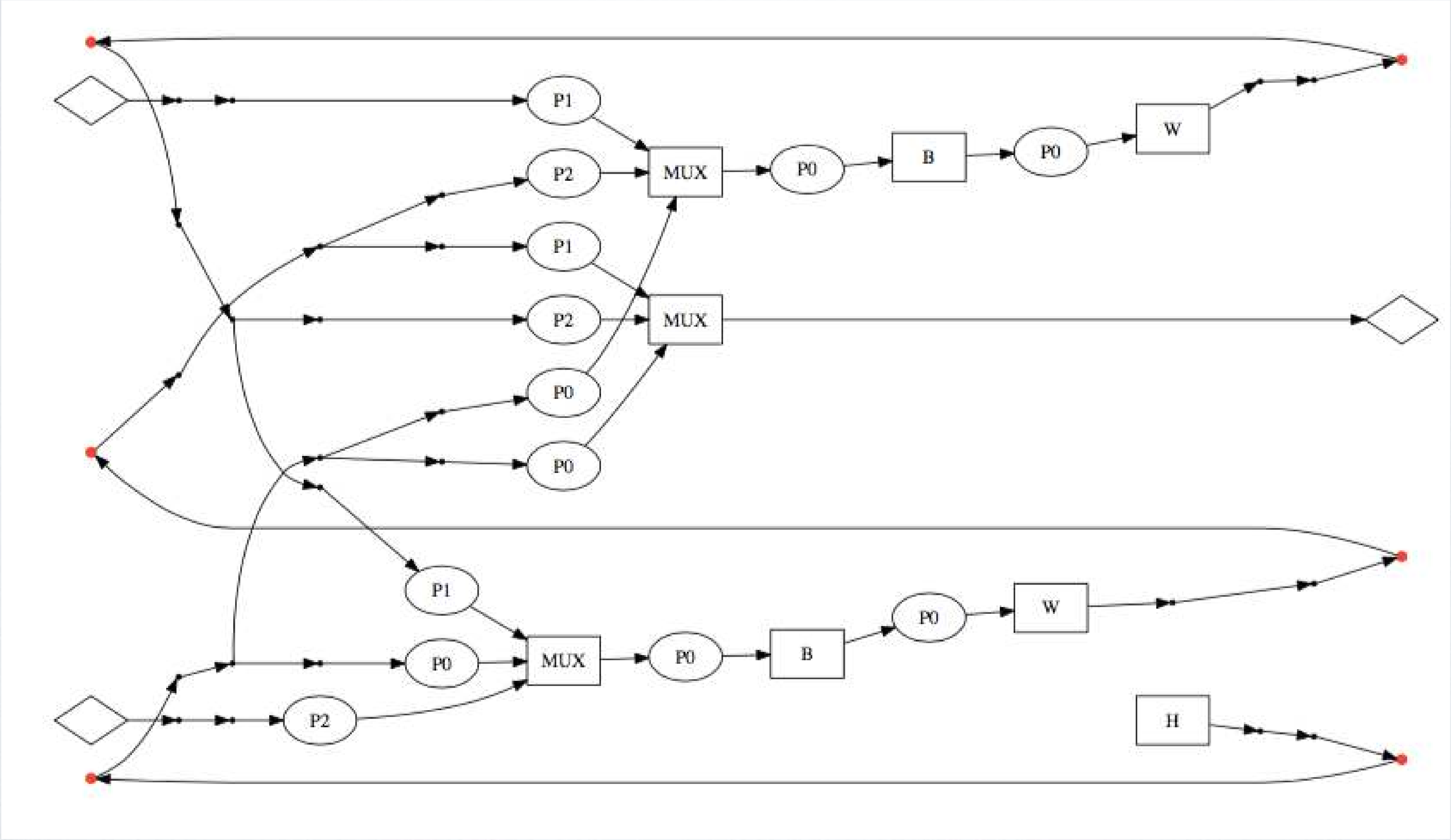
Use equational properties of MUXs (proved elsewhere)

COMBINATIONAL FEEDBACK

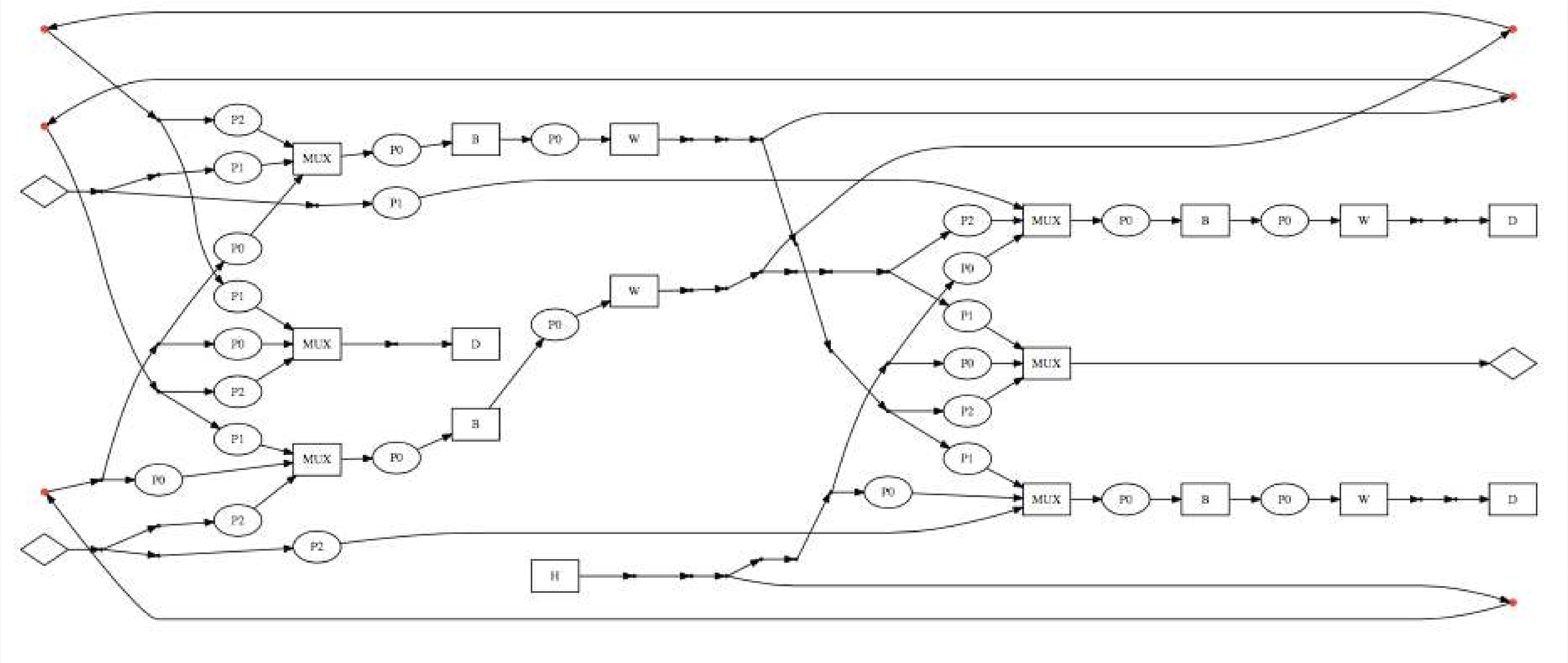


For any (equal) delays (including 0-delays)

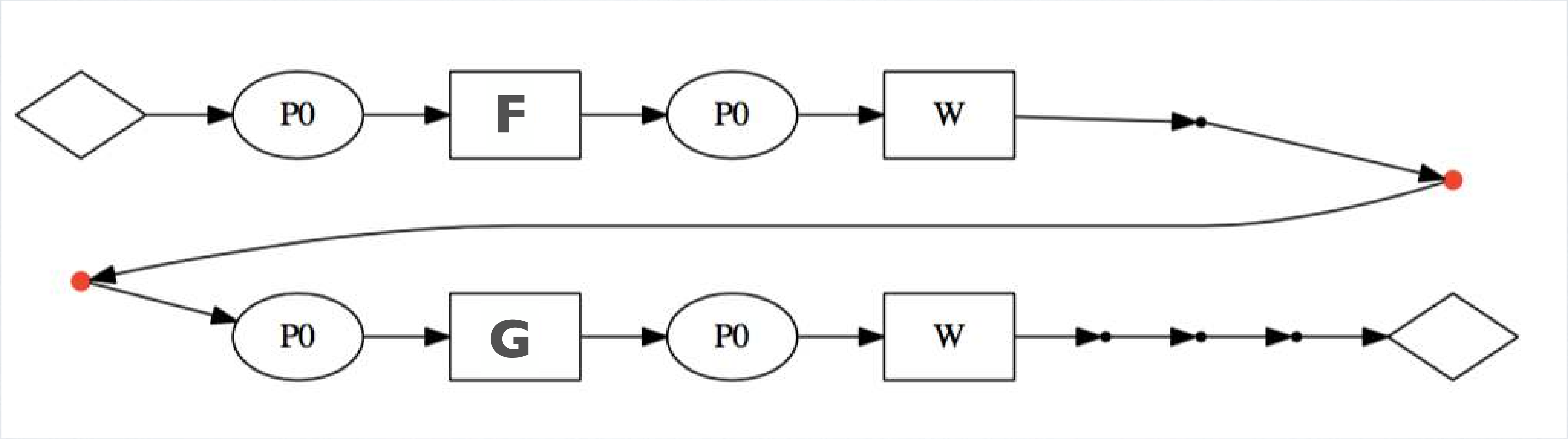
GRAPH REWRITE



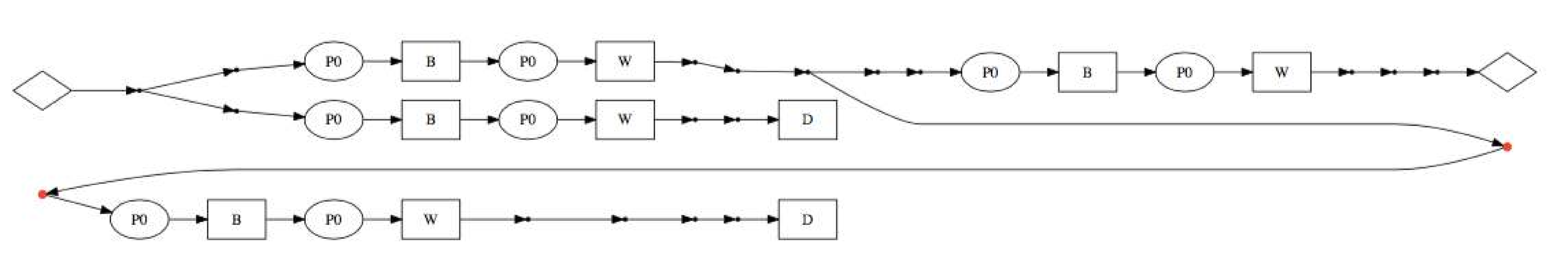
GRAPH REWRITE



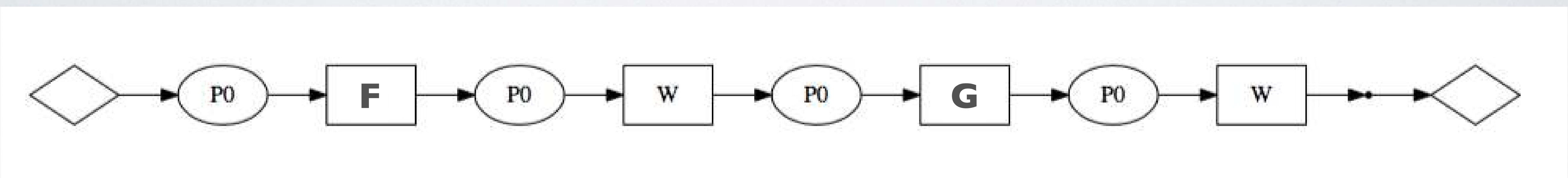
GRAPH REWRITE



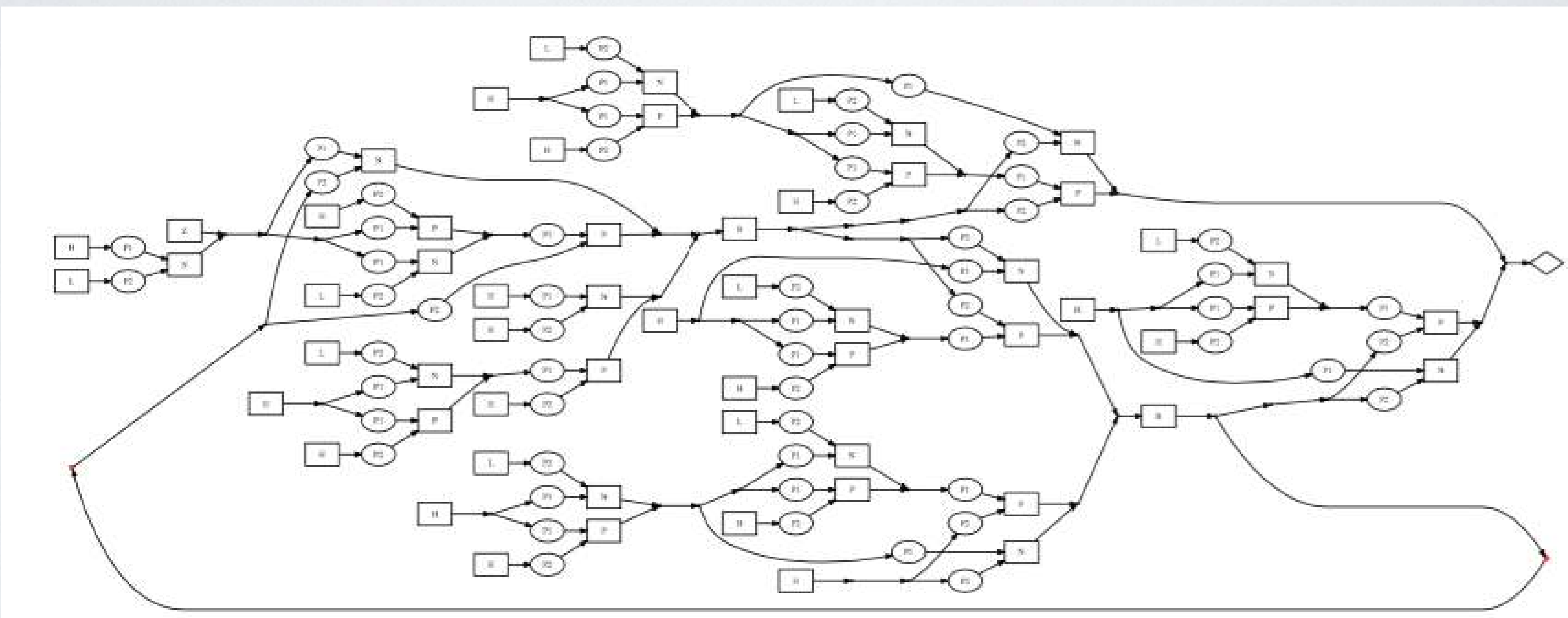
GRAPH REWRITE



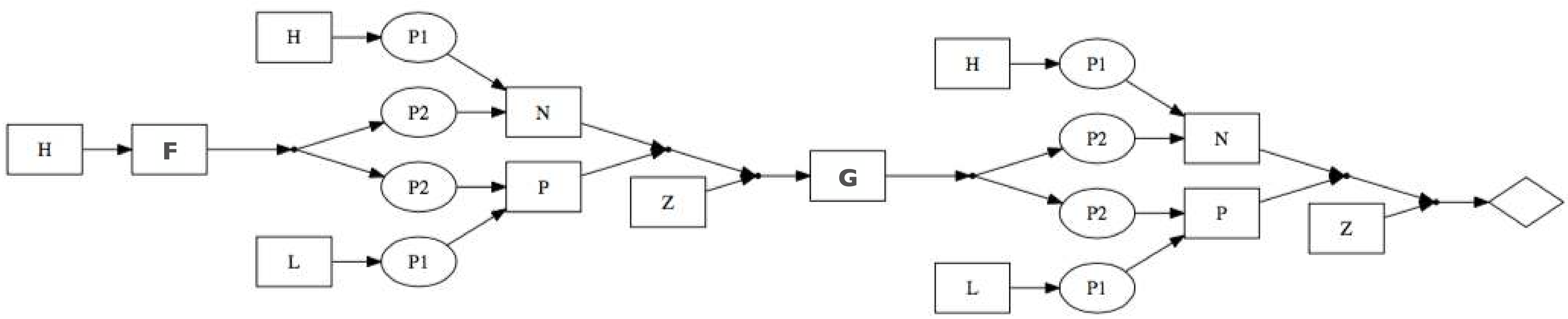
GRAPH REWRITE



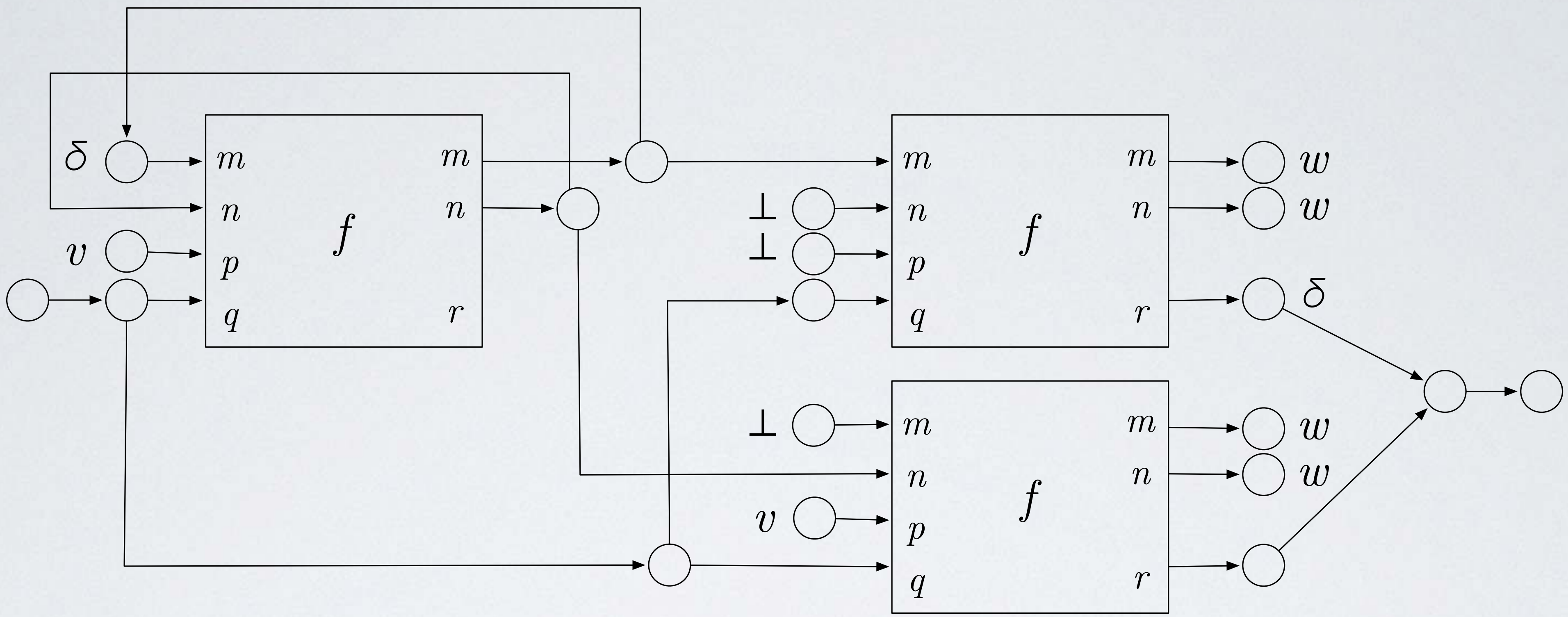
TRANSISTOR-LEVEL (MOSFET)



TRANSISTOR-LEVEL (MOSFET)



▶ **Proposition 16.** Given a graph representing a passified, global trace, global delay circuit, $f : m + n + p + q \to m + n + r$, the following rewrite rule is sound:



▶ **Lemma 17.** A passified, global-trace, global-delay circuit can be unfolded in a time linear in the size of its graph representation.

▶ **Theorem 18.** Closed delay-guarded circuits with no inputs are productive. Given the TPFG representation of a delay-guarded feedback, the rewrite system will produce a TPFG graph representing a circuit $v :: g$ in a finite number of steps.

▶ **Theorem 19.** If a closed, global-trace, global-delay circuit is unproductive after one unfolding then it will always be unproductive.

RELATED WORK

- **HLS** : Sheeran, Luk, Singh, Gill...
- **Denotational Semantics** : Mendler, Shiple, Berry...
- **Diagrammatics** : Kissinger, Coecke, Abramsky...
- **Systems** : Sobocinsky, Zanasi, Bronchi...
- **Category theory** : Baez, Stay, Stefanescu, Hasegawa...

CONCLUSION

- the interplay of **equations** and **diagrams**
- full **automation** of (partial) evaluation
- **compositional** VHDL/Verilog